

TEMPUS JEP 41107-2006 - SYSTEM ON CHIP DESIGN, OVERVIEW OF THE REALIZATION

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Abstract: The TEMPUS JEP 41107 grant was awarded to four Universities. Two of them from the former Yugoslavia (Serbia, University of Niš, Faculty of Electronic Engineering, and Macedonia, Ss. Cyril and Methodius, University of Skopje, Faculty for electronic engineering and computer sciences), and two from the European Union (Spain, Universidad Politecnica de Madrid, and Great Britain, University of Southampton). The main target of the project was the development and implementation (including accreditation) of a new curriculum: "System on chip design". In this paper we will review the activities and the achievements of this project as it comes to an end. Experiences related to implementation and mutual collaboration will be outlined briefly, too.

1. THE SUBJECT AND GOALS OF THE PROJECT

The continuous progress of semiconductor technology has made it possible to implement complex systems on a single chip, which has led to new challenges in design methodologies. Accordingly system on chip (SoC) design has become an advanced professional discipline in modern electronics. Implementing a curriculum in SoC in a developing country such as Serbia or Macedonia means trying to keep the connection with advanced technologies and to give local industry an opportunity to keep pace with the front-running world companies. Reaching this goal needs several requirements to be fulfilled. First, one has to have ambitious departments at the faculties in the developing countries. Second, one needs to establish international collaborations with EU member countries of the appropriate level for transfer of experience and knowledge and with enthusiasm to run for a long period. Finally, one has to produce financial support not only for the staff and student training and retraining but also for investments in new laboratories and publications. All that became possible after the approval of the TEMPUS JEP 41107-2006 project. It was granted for two years (September 2007 – August 2009) but, thanks to some unexpected circumstances has been prolonged until February 2010. The overall amount of support was almost €300,000 unevenly distributed between the partners.

In this short overview of the project we will try to establish a picture, as complete as possible within these four pages, and to give information about all activities related to the project.

2. THE CONSORTIUM

The grant holder of this project is UPM (Universidad Politecnica de Madrid) from Spain with Prof. Octavio Nieto-Taladriz Garcia as the project coordinator from the EU countries' side. The Partner- country-side coordinator is Prof. Vančo Litovski from the University of Niš, Serbia. In addition, the University of Southampton, England, coordinated by Prof. Mark Zwolinski and the Ss Cyril and Methodius University of Skopje, Macedonia, coordinated by Dr. Dimitar Trajanov have taken part in the project. The consortium and this project were established as a new phase in the collaboration between these institutions following collaborations (supported by various European bodies) between some of them for as long as twenty years.

3. THE NEW CURRICULUM

At the University of Niš, the new curriculum that has been developed represents one more phase in the progress of education in the field of CAD of integrated circuits, while at the Ss Cyril and Methodius University the SoC design curriculum is completely a new subject. Introduction of SoC design education in Macedonia represents an outstanding achievement of this project. In Table 1 and Table 2 overviews of both curricula are depicted.

Table 1. System on Chip Design Curriculum Structure at Niš faculty (C = compulsory, E = Elective)

No.	Title	Semester	Credits	Credits	Teaching classes	Exercises
1.	System on chip (C)	IX	4		2	1
2.	Microprocessors and Microsystems (C)	IX	4		2	1
3.	Mixed signal IC design (E)	IX	4		2	2
4.	Design of RF ICs (E)	IX	4		2	2
5.	Intelligent machines (E)	IX	4		2	2
6.	Research and study work		7			
7.	Simulation and optimization of electronic circuits (E)	X		4	2	2
8.	Modelling of electronic circuits and systems (E)	X		4	2	2
9.	Design of Electronic Equipment (E)	X		4	2	2
10.	Research and study work (E)	X		7		
11.	Diploma work	X		18		
	Total		27	33		

The students are required to choose two out of three subjects in the tenth semester.

Table 2. System on Chip Design Curriculum Structure at Skopje faculty

No.	Title	Semester	Credits	Credits	Teaching classes	Exercises
1.	System on chip design techniques	IX	5		2	4
2.	Integrated circuits design	IX	5		2	4
3.	Embedded computer systems software development	IX	5		2	4
4.	Compulsory non-technical course	IX	5		2	4
5.	Specialization elective course	IX	5		2	4
6.	Specialization elective course	IX	5		2	4
7.	Specialization elective course	X		5	2	4
8.	Specialization elective course	X		5	2	4
9.	Master's thesis	X		20		
	Total		30	30		


Following is the full list of the elective courses: Wireless and ad hoc computer networks; Contemporary methods for network analysis; Digital system design using HDL; System reliability; Collaborative computer systems; Digital electronic system design; Custom purpose networks; Cryptography; Process computers; Nanotechnology; and Analogue and mixed signals design.

4. NEW LABORATORIES INSTALLED

Two new SoC design laboratories were established at the respective universities in the partner countries. The value invested in Niš was around €55,000.00 while about €20,000.00 was invested in Skopje. Fig. 1a and Fig. 1b show some of the equipment installed in Niš.



System on Chip Design
(TEMPUS Project JEP 41107_2006)



Objectives of the project

- Develop Electronic integrated circuit design curricula (system on chip) at masters level by coordinating courses.
- Development of laboratory practices and resources to support fabrication and testing.
- Improve students' design improvement.
- Facilitate publishing.

Duration and Budget

- Project start date: 12/2007
- Project end date: 12/2010
- Project budget at EEC2: 400,000 Euro

Project Coordinator at FEEET, Skopje

- Assistant Professor Dr. Zdravko Trajčević, PhD

Participants

- Technical University of Madrid
- Laboratory of Integrated Systems (LIS), Department of Electronic Engineering (DSE), School of Telecommunication Engineering (ETSET)
- University of Southmpton
- Electronic Systems Design Group (ESD), School of Electronics and Computer Science (SES)
- Institute for Core and Peripherals Design
- Department of Informatica and computer science, Faculty of electrical engineering and information technologies (FEEET), University of Niš
- Dalmatian University

Results

Published books

- "System on Chip Design with VHDL"
- "System on Chip Design with SystemC"

New system on chip design curricula at masters level

Laboratory

- Total budget for equipment: 19,870 Euros
- Goal: Build SoC laboratory for computer engineering students laboratory for classes and for research
- Equipment: Server x3, Workstations x7, Tablets/workstations x3, Laboratory equipment x2
- Software: Matlab, NetSOS, Equipment (24x24x16cm LCD, Wireless access point)
- Development tools: (FPGA development boards, The ISE3 Trainer board, Micro-Blaze Development platform, System Development Kit)
- High resolution microscope (SEM, TEM, SEM), Safety and peripheral modules
- Report

Elective courses list at FEEET, Skopje

Course	ECTS	Year	Level
1. System on Chip Design with VHDL	3	2010	Master
2. System on Chip Design with SystemC	3	2010	Master
3. Digital System Design	3	2010	Master
4. Digital System Design	3	2010	Master
5. Digital System Design	3	2010	Master
6. Digital System Design	3	2010	Master
7. Digital System Design	3	2010	Master
8. Digital System Design	3	2010	Master
9. Digital System Design	3	2010	Master
10. Digital System Design	3	2010	Master
11. Digital System Design	3	2010	Master
12. Digital System Design	3	2010	Master
13. Digital System Design	3	2010	Master
14. Digital System Design	3	2010	Master
15. Digital System Design	3	2010	Master
16. Digital System Design	3	2010	Master
17. Digital System Design	3	2010	Master
18. Digital System Design	3	2010	Master
19. Digital System Design	3	2010	Master
20. Digital System Design	3	2010	Master

Figure 1. a) The supercomputer (64 node Beowulf cluster) installed in Niš b) the new SoC design laboratory (eight student working places plus a supervisor's place) and c) a poster presented at the "World day of science for peace and development"

5. STUDENTS AND TEACHERS TRAINING

Within the retraining activities the teachers from Niš spent 5.5 months and the teachers of Skopje spent 2 months at the EU countries' partner universities. At the same time students from Niš spent 11.5 months while students from Skopje 6 months at the EU countries' partner universities. Professors from both EU universities paid visits to both partner countries universities performing retraining locally.

6. PUBLICATIONS AND DISSEMINATION

The following books were published by the respective partner countries faculties:

1. Litovski, V., "Basics of testing of electronic circuits", Niš, 2009.
2. Litovski, V., "Modeling of electronic circuits and systems", Niš, 2009.
3. Petković, P., "Design of CMOS Mixed Signal Integrated Circuits", Niš, 2010.
4. Petković, P., "VHDL and VHDL- AMS support for systems and circuit design", Niš, 2010.
5. Milić, M., Litovski, V., and Andrejević Štosović, M., "Laboratory manual for testing and diagnosis of electronic circuits", Niš, 2010.
6. Andrejević Štosović, M., Milić, M., Mirković, D., and Petković, P., "Laboratory manual for Design of electronic circuits", Niš, 2010.
7. Andrejević Štosović, M., Milić, M., Mirković, D., Petković, P., and Jovanović, B., "Laboratory manual for using Cadence tools for system on chip design", Niš, 2010.
8. Litovski, V., "Solved problems in testing of electronic circuits", Niš, 2010.
9. Trajanov, D., Filiposka, S., Miskovski, I., Grnarov, A., "System on chip Design with SystemC", Skopje, 2010.

10. Trajanov, D., Gramatikov, S., Filiposka, S., and Grnarov, A., "System on chip Design with VHDL", Skopje, 2010.

Seven papers have been published at local [1], national [2-6], and international [7] meetings, promoting the targets and achievements of the project.

A poster illustrating the TEMPUS JEP 41107 2006 project was presented at the "World day of science for peace and development" that took place on November 10, 2009, in the premises of the Ss Cyril and Methodius University in Skopje and is given in Fig. 1c.

Two round tables were organized:

-, "System On Chip Design: Master Studies Experience", The ETRAN 2009 Conference in Vrnjačka banja, June 2009.

-, "SoCD (TEMPUS JEP 41107)", The SSSS 2010 Symposium in Niš, February 2010.

Two web pages related to this project were established and maintained: <http://leda.elfak.ni.ac.rs/tempus> and http://e-tech.feit.ukim.edu.mk/tempus_socd/

The opinions of three experts, working with renowned European R&D microelectronic design centres, about the new curriculum in Niš were collected and published on the web site.

The installation of the new SoC design laboratory in Niš was promoted to the public. A daily newspaper and three local TV stations published the news while the "Zona" TV station broadcasted a 25 minute long interview with Prof. Litovski.

7. FUTURE COLLABORATION AND CONCLUSION

As the best confirmation of excellent collaboration between the partners within this project, we should also consider several applications written for future projects expected to be financed by the TEMPUS or FP7 funds.

Independently of whether new funds will be approved for extension of collaboration between the partners that participated at this project or not, the work implemented and the investment will inevitably have an impact in the education technology of both partner countries' faculties for a long period.

8. REFERENCES

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